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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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THOMAS, KAYDEN, HORSTEMEYER & RISLEY
100 GALLERIA PARKWAY
SUITE 1750
ATLANTA, GA 30339-5948

EXAMINER
KNOLL, CLIFFORD H

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/010,132	WANG ET AL.
	Examiner	Art Unit	
	Clifford H. Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>19 May 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>06 December 2001</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 5/19/05. Currently claims
1-19 are pending.

Claim Rejections - 35 USC § 102

1.   *Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Pekkala*
        (US 2002/0172195).

Regarding claim 1, Pekkala discloses converting native bus signals from a first
computer module to a first point-to-point interface, conveying the bus signals using the
first point-to-point interface to a bus emulator (e.g., paragraph 166), when a bus
emulator is available (e.g., paragraph 165, "on a first-come-first-serve basis"),
conveying the bus signals from the bus emulator using a second point-to-point interface
to a second computer module, and converting the bus signals received at the second
computer to a native form (e.g., paragraph 169).

Regarding claim 2, Pekkala also discloses monitoring the native bus signals in
order to identify the beginning of a data transfer cycle, and accepting data and address
signals from the native bus and serializing these (e.g., paragraph 8), together with an
indication of the type of transfer identified (e.g., paragraph 166).

Regarding claim 3, Pekkala also discloses receiving the bus signals from the first

point-to-point interface in the bus emulator; translating the first point-to-point interface

received in the bus emulator to a bus structure internal to the bus emulator; conveying

the bus signals received in the bus emulator by way of the first point-to-point interface

onto said bus structure (e.g., paragraph 166); and translating the bus signals carried on

said bus structure to a second point-to-point interface (e.g., paragraph 55).

Regarding claim 4, Pekkala also discloses granting said bus structure to the first

point-to-point interface if said bus structure is available; and propagating the bus signals

translated from the first point-to-point interface onto the bus structure if the bus structure

is granted to said first point-to-point interface (e.g., paragraph 150).

Regarding claim 5, Pekkala discloses plurality of point-to-point interface units

comprising a computer module interface and a point-to-point interface; plurality of

computer modules connected to the computer module interface of the plurality of point-

to-point interface units; and bus emulator connected to the point-to-point interface of

the plurality of point-to-point interface units (e.g., paragraph 55), the emulator capable of

supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI

buses on a host 102 rather than PCI buses 216 in an I/O unit 108").

Regarding claim 6, Pekkala also discloses the point-to-point interface units

comprise parallel-to-serial conversion units that operate upon detecting the beginning of

a data transfer cycle presented to the computer module interface (e.g., paragraph 8),

and wherein the parallel-to-serial conversion units accept a data field and an address

field and a cycle-type indicator from the computer module interface (e.g., paragraph 166).

Regarding claim 7, Pekkala also discloses the plurality of point-to-point interface units comprise high-current parallel drivers (e.g., paragraph 10, "multiple IB channel adapters") capable of propagating data, address and data transfer cycle requests (e.g., paragraph 166).

Regarding claim 8, Pekkala also discloses the plurality of point-to-point interfaces interconnected by an internal bus (e.g., paragraph 9).

Regarding claim 9, Pekkala also discloses the arbiter for granting access to the internal bus to one of the plurality of point-to-point interfaces (e.g., paragraph 150).

Regarding claim 10, Pekkala also discloses a cascade port that connects to the internal bus and can be used to extend the length of the internal bus (e.g., paragraph 10).

Regarding claim 11, Pekkala discloses a point-to-point interface (e.g., paragraph 8) , the emulator capable of supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI buses on a host 102 rather than PCI buses 216 in an I/O unit 108").

Regarding claim 12, Pekkala also discloses parallel-to-serial conversion unit that operate upon detecting the beginning of a data transfer cycle presented to the computer module interface (e.g., paragraph 8), and wherein the parallel-to-serial conversion units accept a data field and an address field and a cycle-type indicator from the computer

module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface (e.g., paragraph 166).

Regarding claim 13, Pekkala also discloses the point-to-point interface comprises high-current parallel drivers capable of propagating data, address and data transfer cycle requests (e.g., paragraph 10).

Regarding claim 14, Pekkala discloses a computer module interface and a point-to-point interface (e.g., paragraph 9) , the emulator capable of supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI buses on a host 102 rather than PCI buses 216 in an I/O unit 108").

Regarding claim 15, Pekkala also discloses parallel-to-serial conversion unit that operate upon detecting the beginning of a data transfer cycle presented to the computer module interface (e.g., paragraph 8), and wherein the parallel-to-serial conversion units accept a data field and an address field and a cycle-type indicator from the computer module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface (e.g., paragraph 166).

Regarding claim 16, Pekkala also discloses the plurality of point-to-point interface units comprise high-current parallel drivers capable of propagating data, address and data transfer cycle requests (e.g., paragraph 10).

Regarding claim 17, Pekkala discloses an internal bus; and plurality of point-to-point interfaces interconnected by the internal bus (e.g., paragraph 8, "IBA"), , the emulator capable of supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI buses on a host 102 rather than PCI buses 216 in an I/O unit 108").

Regarding claim 18, Pekkala also discloses an arbiter for granting access to the

internal bus to one of the plurality of point-to-point interfaces (e.g., paragraph 150).

Regarding claim 19, Pekkala also discloses a cascade port connected to the

internal bus and can be used to extend the length of the internal bus (e.g., paragraph

10).

Response to Arguments

Applicant's arguments filed 3/19/05 have been fully considered but they are not

persuasive.

Applicant makes inference that Office Action suggests "ability of the bus emulator

to support a single transaction at a time" can distinguish over the art (p. 8); however, in

the Advisory Action of 2/14/05, Examiner states that this feature raises new issues.

Specifically, Examiner determined that the new feature distinguished over the art of

record as it was currently applied. In the instant Office Action, Examiner has

determined that an additional interpretation of the art of record has established this

feature as anticipatory. The new interpretation is applied supra.

Applicant argues that the bus emulator of the claimed invention is distinct from

Pekkala's transaction switch (p. 8); however, the distinction is not supported in the

claims. As it is recited, Pekkala's transaction switch is seen to teach precisely the

feature of the bus emulator as it is claimed.

Applicant further argues that the bus emulator "includes an internal bus with which all point-to-point interfaces are communicatively coupled to. As such, this internal bus really is a bus where only one transfer can be accommodated at any given time" (pp. 8-9); however, as this new feature is recited as "wherein the bus emulator is capable of supporting only one transfer at a time". It is determined above that Pekkala to is capable of supporting a single transaction at a time. At the cited passage, it is clear that it is possible for only one bus to be connected, from which one may conclude its capability of supporting only one transfer.

Applicant further argues that Pekkala can be characterized as a network switch where data is passed concurrently. In distinction, Applicant claims that "[a]s Applicant claims, the bus emulator is a bus that can have contention as different point-to-point interfaces vie for access to the bus" (p. 9); however these features are not claimed. The recitation as it stands is anticipated by Pekkala; Applicant may consider adding additional features to support this distinction, if this is what is intended as the claimed invention.

Applicant further argues that Pekkala discloses a "transfer switch" and "not a bus as Applicant has taught" (p. 9); however, the claims do not limit the interpretation of the "bus emulator" as a bus. In fact, the feature relied upon by Pekkala is not the capability to switch per se, but rather the fact that PCI signals are converted to a format within the transfer switch and passed to another point where it is converted to a native format, possibly the same native format as the input format, as appropriate. As Pekkala takes

signals from a bus and faithfully transfers them to another location intact, Examiner finds that Pekkala can be interpreted as a bus emulator.

Applicant further argues that Pekkala does not disclose "converting received bus signals to a native form" (p. 10); however, at the cited passage, Pekkala "detects the modified transaction" and "transfers the addressed data on its PCI bus" (paragraph 169). Examiner interprets the PCI protocol as a native format.

Regarding claim 2, Applicant argues that Pekkala does not disclose "monitoring native bus cycles" (p. 10); however, at the cited passage Pekkala discloses that the interface has "written the addressed data to the allocated buffer" and posts an addressed data transaction" (paragraph 166); Examiner finds that these operations constitute the monitoring of bus signals because of the operations which are responsive to monitoring. The other cited passage (paragraph 8) supports the feature of serializing, which is performed in Pekkala's IB switch.

Regarding claim 3, Applicant argues that Pekkala does not disclose "reception of bus signals from a first point-to-point interface in the bus emulator"; however, at the cited passage clearly discloses receiving bus signals from a PCI interface (paragraph 166). The Examiner interprets the bus structure as claimed as a feature that renders the bus signals intact from one point to another point. The claim does not recite a particular bus, but rather recites "bus emulator" and "bus structure"; therefore, the requirements of the interpretation are to disclose an emulator and a structure, which are for a bus. Examiner finds Pekkala discloses these features.

Regarding claim 4, Applicant argues that Pekkala does not disclose "propagating signals onto the bus if the bus structure is granted to the point-to-point interface" (p. 10); however, a bus as defined is the transmission of signals from one point to another point. Pekkala discloses the transmission of signals from the output queue to the PCI bus from the PCI I/F (paragraphs 149-150).

Applicant further argues that there is "no mention of arbitration"; however, arbitration is not claimed. A "granting... if said bus structure is available"; however, Pekkala's bus structure grants use of the bus structure "on a first-come-first-serve basis" (paragraph 165).

Regarding claims 7, 13, and 16, Applicant argues that Pekkala does not disclose the "high-current driver" (p. 11); however, at the cited passage Pekkala discloses the extension of the internal bus by use of multiple IB switches to allow greater interconnection among devices (e.g., paragraph 10). The external connection will necessarily constitute a driver to drive the signal beyond current required for internal use. Any distinction is not supported.

Regarding claims 8 and 17, Applicant argues that an internal bus is not disclosed by Pekkala (pp. 11, 12), however, as treated supra, Pekkala transmits data from one point to another point; this action is the definition of a bus.

Regarding claims 9 (and 18), Applicant argues that "arbitration and granting" ("use of an arbiter", pp. 11, 12) are not disclosed in Pekkala; however this argument is treated supra with respect to claim 4.

Regarding claims 10 and 19, Applicant argues that Pekkala does not disclose "a cascade port to extend an internal bus" (p. 11, 12); however, Pekkala uses a cascade of IB switches to extend to interconnection beyond the immediate devices connected to any given switch (e.g., paragraph 10).

Regarding claim 15, Applicant argues that Pekkala does not disclose "a serial output is generated once a data field and an address field are accepted; however at he cited passage Pekkala discloses the IB packet format which is a serial format. Pekkala uses this packet format to transmit data and address field information received from the input queue of the PCI buses.

Applicant argues that the claimed invention is a method and apparatus "that enables extension and distal interaction of computer modules on a cycle-by-cycle basis" (p. 12); however, to the extent that this is recited, Pekkala is determined to anticipate the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Business Center (EBC) at 866-217-9197 (toll-free).

chk

**TIM VO
PRIMARY EXAMINER**